OpenCores.Org

SPDIF Specification

Author: Geir Drange
gedra@opencores.org

WISHBONE COMPATIBLE

Rev. 1.5
July 21, 2004

This page has been intentionally left blank.

Revision History

Rev.	Date	Author	Description
0.1	30/4/04	Geir Drange	First Draft
1.0	15/5/04	Geir Drange	Updated
1.1	13/6/04	Geir Drange	Renamed generics and modified receiver configuration register
1.2	26/6/04	Geir Drange	Corrected a few typo's.
1.3	15/7/04	Geir Drange	Changed two interrupts in transmitter
1.4	19/7/04	Geir Drange	Corrected some typo's
1.5	21/7/04	Geir Drange	Final corrections before release.

Contents

1 Introduction

The SPDIF (or AES/EBU, IEC950 standards) is a point-to-point protocol for serial transmission of digital audio through a single transmission line. The transmission medium can be either electrical or optical (e.g. TosLink). It provides two channels for audio data, a method for communicating control information, and some error detection capabilities. The control information is transmitted as one bit per sample and accumulates in a block structure. The data is bi-phase encoded, which enables the receiver to extract a clock from the data. Coding violations, defined as preambles, are used to identify sample and block boundaries.

SPDIF interfaces are found on most CD/DVD players, audio equipment and computer sound cards.

2

Architecture

The SPDIF interface consists of two separate cores, a transmitter and a receiver

2.1 SPDIF Receiver

The receiver architecture is shown below.

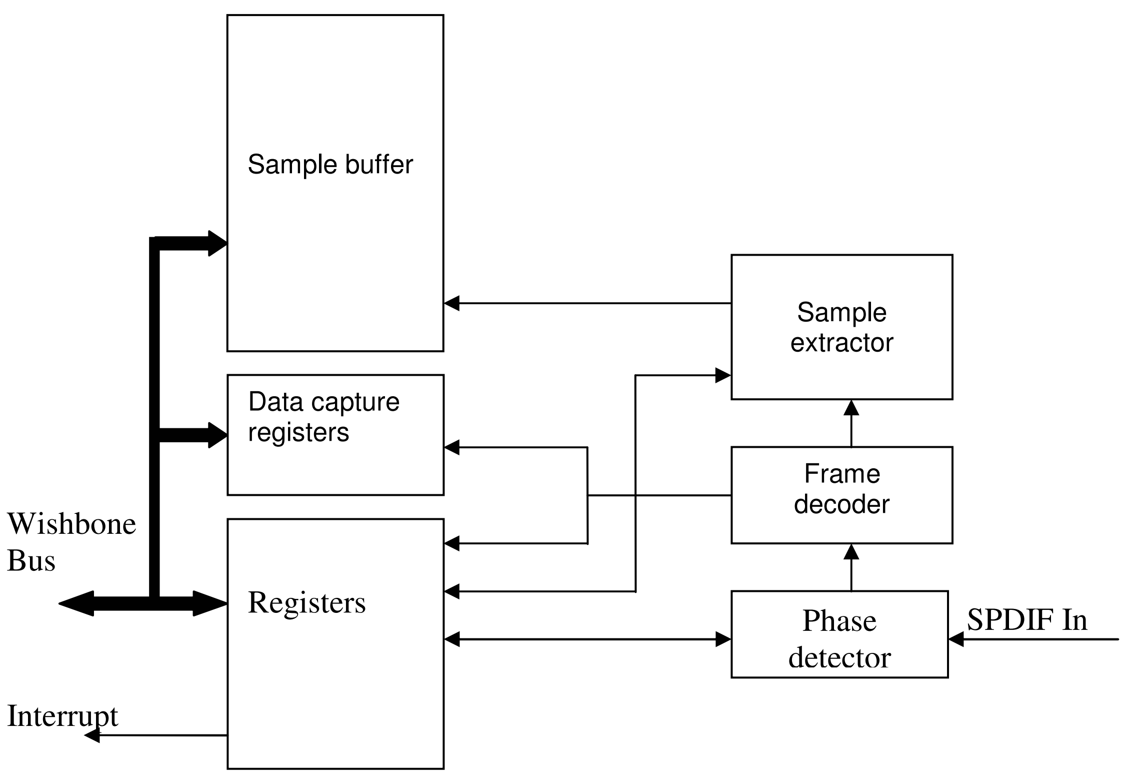

Figure 1: Receiver Block Diagram

The bi-phase encoded SPDIF signal is decoded by an oversampling phase detector. The wishbone bus clock is used to sample the input signal, and must be at least 8 times higher than then SPDIF data rate. The lowest SPDIF bit-rate supported is 100kHz.

A frame decoder locks onto the code violations (preambles) that mark the start of frames and sub-frames. Audio data is extracted and placed into the sample buffer. The size of the sample buffer is determined by the Wishbone address bus width. Minimum sample buffer size is 128bytes. The sample buffer is addressed by setting the most significant address bit to '1'. The sample buffer is divided in two equal parts, lower and upper, and the user will be notified when either is filled with audio data.

Sub-frame status bits can optionally be included in the sample buffer.

2.2 SPDIF Transmitter

The transmitter architecture is shown below.

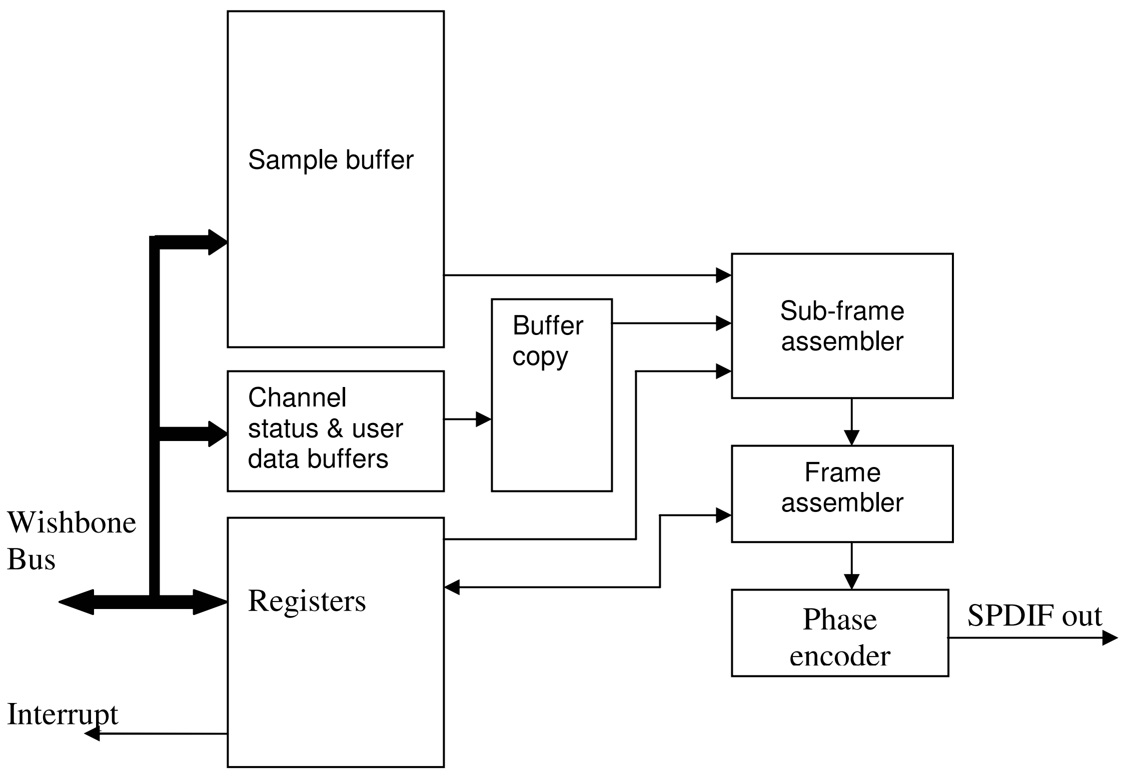

Figure 2: Transmitter Block Diagram

The sub-frame assembler creates 32bit data words from sample data, register settings and optionally channel status/user data buffers. A parity bit is added in each sub-frame. The frame assembler adds preambles to create a frame of two sub-frames. 192 frames add up to a block. The block structure is bi-phase encoded before transmitting.

The size of the sample buffer is determined by the Wishbone address bus width. Minimum sample buffer size is 128bytes. The sample buffer is addressed by setting the most significant address bit to '1'. The sample buffer is divided in two equal parts, lower and upper, and the user will be notified when either is emptied of audio data.

Channel status can be generated from a dedicated 192bit buffer. Two interrupts can be generated when the transmitter reads from the buffer, one in the middle and one at the end. The user data buffer operates in an identical way.

3

Operation

This chapter contains operational guidelines for the cores.

3.1 Receiver

Some features are not available when the core is synthesized in 16bit mode.

3.1.1 Resetting

Except for the Wishbone reset, the receiver can be disabled by clearing the RXEN bit in the RxConfig register.

3.1.2 Capture registers

Before the receiver is enabled, the capture registers should be set up to capture bit-fields of interest, like sample frequency (bit 24-27 in consumer mode).

3.1.3 Enable receiver

Set RXEN bit in RxConfig register to enable the receiver. Then wait until the LOCK bit is set in the RxStatus Register. Examine the other status bits in RxStatus register to identify the type of signal being received, and set up the other bits in the RxConfig register. Finally set the SAMPLE bit to start data transfer to the sample buffers.

3.1.4 Transferring data

The best way to read out data is to set up an interrupt to be generated when the lower or upper buffer is full, and then execute a block read of the data.

3.2 Transmitter

3.2.1 Resetting

Except for the Wishbone reset, the transmitter can be disabled by clearing the TXEN bit in the TxConfig register

3.2.2 Selecting transmit data rate

The data rate of the SPDIF signal is a function of the Wishbone bus clock and the RATIO bits in the TxConfig register. The bit rate is 64 times the sampling frequency – each sample is encoded as 32bits and there are two channels. Sample frequency is given by the following equation:

$$S_{freq} = \frac{Wishbone\_clock\_frequency}{128 \cdot (RATIO + 1)}$$

Example: Data rate is 48kHz and Wishbone clock frequency is 12.288MHz. The RATIO bits must then be set to 1. Output data rate is 3.072Mbps.

3.2.3 Selecting data format

If the Wishbone data bus is 16bit, it is only possible to send 16bit audio data. In 32bit mode, any sample resolution from 16 to 24bit can be transmitted. Data format is selected by the MODE bits in the TxConfig register.

3.2.4 Setting up channel status bits

If output format is standard consumer audio, set CHSTEN to 0 in TxConfig, and set TxChStat to desired format. Otherwise set up the ChStatus buffer with desired channel status data (192bits). If the channel status bits are not changing from block to block, it is only necessary to program the buffer once. Otherwise the HCSBF/LCSBF bits in TxIntMask must be set, and the buffer will need to be updated for every half block transmitted.

3.2.5 Setting up user data bits

User data bits are normally set to zero, but if required user data can be transmitted using the UserData buffer. If the user data bits are not changing from block to block, it is only necessary to program the buffer once. Otherwise the HCSBF/LCSBF bits in TxIntMask must be set, and the buffer will need to be updated for every block.

3.2.6 Preparing sample buffer

Before the TXDATA bit in TxConfig is set, fill up the complete sample buffer with audio data. The transmitter will generate an interrupt when lower half or upper half of sample buffer is emptied,

3.2.7 Start transmission

Transmission of SPDIF signal starts when the TXEN bit in TxConfig is set. If TXDATA bit is not set, the transmitted data will be all zeroes with the sub-frame validity bit set.

Once the TXDATA bit is set, audio data from the sample buffer will be transmitted and the validity bit is cleared.

4

Generics

The SPDIF interface has a number of generics that can be used to tailor the interface for various needs.

4.1 Generics for both transmitter and receiver

Name	Type	Range	Description
DATA_WIDTH	Integer	16/32	Wishbone data bus width. If using 16bit bus, some functionality is lost.
ADDR_WIDTH	Integer	8 - 64	Wishbone addresses bus width. The sample buffer occupies half the address range.

Table 1: Generics for transmitter and receiver

4.2 Generics for the receiver

Name	Type	Range	Description
CH_ST_CAPTURE	Integer	0 – 8	Specifies the number of channel status capture registers. Only applicable in 32bit mode.
WISHBONE_FREQ	Natural	1 -	WishBone bus frequency in MHz.. This generic is used to optimize the phase detector.

Table 2: Generics for receiver

4.3 Generics for the transmitter

Name	Type	Range	Description
USER_DATA_BUF	Integer	0 – 1	0: No user data buffer is generated 1: User data buffer is generated
CH_STAT_BUF	Integer	0 – 1	0: No channel status data buffer is generated 1: Channel status data buffer is generated

Table 3: Generics for transmitter

5

Registers

This section specifies all internal registers of the SPDIF interface.

5.1 SPDIF Receiver

5.1.1 Receiver registers - overview

Name	Address	Width	Access	Description
RxVersion	0x00	16/32	R	Version register
RxConfig	0x01	16/32	RW	Configuration register
RxStatus	0x02	16/32	R	Signal Status Register
RxIntMask	0x03	16/32	RW	Interrupt mask register
RxIntStat	0x04	16/32	RW	Interrupt status register
The following registers are optional depending on the value of **CH_ST_CAPTURE**				
ChStCap0	0x10	32	RW	Channel status capture register 0
ChStData0	0x11	32	R	Channel status data register 0
ChStCap1	0x12	32	RW	Channel status capture register 1
ChStData1	0x13	32	R	Channel status data data register 1
ChStCap2	0x14	32	RW	Channel status capture register 2
ChStData2	0x15	32	R	Channel status data data register 2
ChStCap3	0x16	32	RW	Channel status capture register 3
ChStData3	0x17	32	R	Channel status data data register 3
ChStCap4	0x18	32	RW	Channel status capture register 4
ChStData4	0x19	32	R	Channel status data data register 4
ChStCap5	0x1a	32	RW	Channel status capture register 5
ChStData5	0x1b	32	R	Channel status data data register 5
ChStCap6	0x1c	32	RW	Channel status capture register 6
ChStData6	0x1d	32	R	Channel status data data register 6
ChStCap7	0x1e	32	RW	Channel status capture register 7
ChStData7	0x1f	32	R	Channel status data data register 7

Table 4: Receiver registers

5.1.2 RxVersion – Description

The version register allows the SW to read out all the parameter that's was used to generate the receiver.

Bit #	Access	Name	Description
31-20	R	-	Unused
19-16		CAPNO	The value of **CH_ST_CAPTURE**
15-12		-	Unused
11-5		ADRW	The value of **ADDR_WIDTH**
4		DATW	0: **DATA_WIDTH** is 16bit 1: **DATA_WIDTH** is 32bit
3-0		VER	SPDIF Version number = 1

Reset Value:

RxVersion: Depends on generics

5.1.3 RxConfig – Description

The configuration register controls the operation of the receiver.

Bit #	Access	Name	Description
31-25	R	-	Unused
24	RW	BLKEN	0: Do not use block boundary marking 1: Mark the first sample in each block with a 1 in bit 27.
23-20	RW	MODE	0: Store samples as 16bit 1: Store samples as 17bit 2: Store samples as 18bit 3: Store samples as 19bit 4: Store samples as 20bit 5: Store samples as 21bit 6: Store samples as 22bit 7: Store samples as 23bit 8: Store samples as 24bit 9-15: Reserved
19		PAREN	0: Do not store parity bit 1: Store parity bit in bit 31 in sample buffer
18		STATEN	0: Do not store channel status bit 1: Store channel status bit in bit 30 in sample buffer
17		USEREN	0: Do not store user data bit 1: Store user data bit in bit 29 in sample buffer
16		VALEN	0: Do not store validity bit 1: Store validity bit in bit 28 in sample buffer
15-5	R	-	Unused

Bit #	Access	Name	Description
4	RW	VALID	0: Sample data stored in buffers regardless of sub-frame Validity bit 1: Sample data stored only when sub-frame Validity bit is 0
3		CHAS	0: RxStatus register holds status from channel B 1: RxStatus register holds status from channel A
2		RINTEN	0: Interrupt output is disabled 1: Interrupt output is enabled
1		SAMPLE	0: No data is stored in the sample buffer 1: Data is stored in the sample buffer
0		RXEN	0: Receiver is disabled 1: Receiver is enabled

Reset Value:

RxConfig: 0x0000

5.1.4 RxStatus – Description

The signal status register holds information about the received signal. When the receiver is disabled, all bits read 0. When lock bit is 0, all other bits are set to 0.

Bit #	Access	Name	Description
31-16	R	-	Unused
15-7		-	Unused
6		COPY	0: Copy inhibited 1: Copy permitted (copy bit only applicable in consumer mode)
5-3		EMPH	Emphasis code from the channel status block. Note that the interpretation of these bits is different in consumer and professional mode.
2		AUDIO	0: Signal is non-audio 1: Signal is audio
1		PRO	0: Signal format is consumer 1: Signal format is professional
0		LOCK	0: Receiver has no valid input signal 1: Receiver is locked to SPDIF signal

Reset Value:

RxStatus: 0x0000

5.1.5 RxIntMask – Description

Set bit to 1 in the mask register to enable an interrupt source.

Bit #	Access	Name	Description
31-16	R	-	Unused
23	RW	CAP7	Capture register 7 interrupt mask

Bit #	Access	Name	Description
22		CAP6	Capture register 6 interrupt mask
21		CAP5	Capture register 5 interrupt mask
20		CAP4	Capture register 4 interrupt mask
19		CAP3	Capture register 3 interrupt mask
18		CAP2	Capture register 2 interrupt mask
17		CAP1	Capture register 1 interrupt mask
16		CAP0	Capture register 0 interrupt mask
15-5	R	-	Unused
4	RW	PARITYB	Parity error channel B interrupt mask
3		PARITYA	Parity error channel A interrupt mask
2		HSBF	Higher sample buffer full interrupt mask
1		LSBF	Lower sample buffer full interrupt mask
0		LOCK	Change in lock bit interrupt mask

Reset Value:

RxIntMask: 0x0000

5.1.6 RxIntStat – Description

A bit in this register is set to 1 when an event occurs. If the corresponding bit in RxIntMask is set to 1, an interrupt is generated (if enabled). Write a 1 to a bit to clear the event. The interrupt signal goes inactive when all events have been cleared.

Bit #	Access	Name	Description
31-24	R	-	Unused
23	RW	CAP7	Capture register 7 changed
22		CAP6	Capture register 6 changed
21		CAP5	Capture register 5 changed
20		CAP4	Capture register 4 changed
19		CAP3	Capture register 3 changed
18		CAP2	Capture register 2 changed
17		CAP1	Capture register 1 changed
16		CAP0	Capture register 0 changed
15-5	R	-	Unused
4	RW	PARITYB	Parity error detected on channel B
3		PARITYA	Parity error detected on channel A
2		HSBF	Higher sample buffer full
1		LSBF	Lower sample buffer full
0		LOCK	Change in lock bit in RxStatus register

Reset Value:

RxIntStat: 0x0000

5.1.7 ChStCap<n> – Description

The channel status capture register can be set up to capture a specified bit-field of the channel status frame or user data frame, and also generate an interrupt when the bit-field changes. The bit-field can be from 1 to 32 bits long. There can be up to eight sets of bit-field capture registers.

Bit #	Access	Name	Description
31-16	R	-	Unused
15-8	RW	BITPOS	First bit position of bit-field to be captured Valid range is 0 to 191
7	RW	CDATA	0: User data is captured 1: Channel status data is captured
6	RW	CHID	0: Source is channel A 1: Source is channel B
5-0	RW	BITLEN	0: Capture function disabled 1-32: Length of bit-field to be captured

Reset Value:

ChStCap: 0x0000

5.1.8 ChStData<n> – Description

Captured channel status/user data bits.

Bit #	Access	Name	Description
31-0	R	DATA	Captured channel status. First bit captured is stored in bit 0.

Reset Value:

ChStData: 0x0000

5.1.9 Receive sample data – Description

Format of data words in receive sample buffer

Bit #	Access	Name	Description
31	R	PARITY	Parity bit (if enabled, otherwise 0)
30		CHSTAT	Channel status bit (if enabled, otherwise 0)
29		USRDAT	User Data bit (if enabled, otherwise 0)
28		VALID	Validity bit (if enabled, otherwise 0)
27		BLKSTART	Start of sample block bit (if enabled, otherwise 0)
26-24		-	Unused
23-16		DATH	Audio data if >16bit resolution. Unused bits are 0
15-0		DATL	Audio data. Bit 0 is LSB.

Reset Value:

Sample buffer: undefined

5.2 SPDIF Transmitter

5.2.1 Transmitter registers - overview

Name	Address	Width	Access	Description
TxVersion	0x00	16/32	R	Version register
TxConfig	0x01	16/32	RW	Configuration register
TxChStat	0x02	16/32	RW	Channel status control register
TxIntMask	0x03	16/32	RW	Interrupt mask register
TxIntStat	0x04	16/32	RW	Interrupt status register
The following registers are optional depending on the value of **USER_DATA_BUF**				
UserData	0x20-0x37	16/32	W	User data buffer
The following registers are optional depending on the value of **CH_STAT_BUF**				
ChStatus	0x40-0x57	16/32	W	Channel status buffer

Table 5: Transmitter registers

5.2.2 TxVersion – Description

The version register allows the SW to read out all the parameter that's was used to generate the transmitter.

Bit #	Access	Description
31-14	R	Unused
13	R	0: Channel status buffer not available 1: Channel status buffer available
12	R	0: User data buffer not available 1: User data buffer available
11-5	R	The value of **ADDR_WIDTH**
4	R	0: **DATA_WIDTH** is 16bit 1: **DATA_WIDTH** is 32bit
3-0	R	SPDIF Version number = 1

Reset Value:

TxVersion: -

5.2.3 TxConfig – Description

The configuration register controls the operation of the transmitter. When **DataWidth**=16, only 16bit samples can be transmitted.

Bit #	Access	Name	Description

Bit #	Access	Name	Description
31-24	R	-	Unused
23-20	RW	MODE	Sample format: 0: 16bit 1: 17bit 2: 18bit 3: 19bit 4: 20bit 5: 21bit 6: 22bit 7: 23bit 8: 24bit 9-15: Reserved
19-16	R	-	unused
15-8	RW	RATIO	Clock divider for the transmit frequency. The Wishbone bus clock is divided by a factor of (1+RATIO) to generate the serial transmit clock.
7-6		UDATEN	0: User data A&B set to 0. 1: User data A&B generated from UserData bit 7-0 2: User data A generated from UserData bit 7-0, B generated from UserData bit 15-8 3: reserved
5-4		CHSTEN	0: Channel status A&B generated from TxChStat 1: Channel status A&B generated from ChStat bit 7-0 2: Channel status A generated from ChStat bit 7-0, B generated from ChStat bit 15-8 3: reserved
3	R	-	unused
2	RW	TINTEN	0: Interrupt output is disabled 1: Interrupt output is enabled
1		TXDATA	0: Data from buffer not transmitted (validity bit set to 1) 1: Data from buffer transmitted (validity bit set to 0)
0		TXEN	0: Transmitter is disabled 1: Transmitter is enabled

Reset Value:

TxConfig: 0x0000

5.2.4 TxChStat – Description

The transmit channel status register can be used to set the most important bits of the 192bit channel status frame when the channel status buffer is not enabled. This register only applies to consumer mode. Professional mode requires the channel status buffer.

Bit #	Access	Name	Description
31-8	R	-	Unused

Bit #	Access	Name	Description
7-6	RW	FREQ	Sample frequency: 00: 44.1kHz 01: 48kHz 10: 32kHz 11: Sample rate converter
5-4	R	-	unused
3	RW	GSTAT	Generation status: (category code is set to 00) 0: No Indication 1: Original/commercially pre-recoded data
2	RW	PREEM	Pre-emphasis: 0: None 1: 50/15us
1	RW	COPY	Copyright: 0: Copy inhibited 1: Copy permitted
0	RW	AUDIO	Data format: 0: Audio 1: Non-audio

Reset Value:

TxChStat: 0x0000

5.2.5 TxIntMask – Description

Set bit to 1 in the mask register to enable an interrupt source.

Bit #	Access	Name	Description
31-16	R	-	Unused
15-5	R	-	Unused
4	RW	HCSBF	Higher channel status/user data buffer empty
3		LCSBF	Lower channel status/user data buffer empty
2		HSBF	Higher sample buffer empty
1		LSBF	Lower sample buffer empty
0	R	-	Unused

Reset Value:

TxIntMask: 0x0000

5.2.6 TxIntStat – Description

A bit in this register is set to 1 when an event occurs. If the corresponding bit in TxIntMask is set to 1, an interrupt is generated (if enabled). Write a 1 to a bit to clear the event. The interrupt signal goes inactive when all events have been cleared.

Bit #	Access	Name	Description
31-16	R	-	Unused

Bit #	Access	Name	Description
15-5	R	-	Unused
4	RW	HCSBF	Higher channel status/user data buffer empty
3		LCSBF	Lower channel status/user data buffer empty
2		HSBF	Higher sample buffer empty
1		LSBF	Lower sample buffer empty
0	R	-	Unused

Reset Value:
TxIntStat: 0x0000

5.2.7 UserData – Description

The user data is 24 bytes per sample block. Bit 0 of byte 0 is transmitted first. Bit 7 of byte 23 is transmitted last.

Bit #	Access	Name	Description
31-16	-	-	Unused
15-8	W	CHBUD	Channel B user data
7-0		CHAUD	Channel A user data

Reset Value:
UserData: undefined

5.2.8 ChStat – Description

The channel status data is 24 bytes per sample block. Bit 0 of byte 0 is transmitted first. Bit 7 of byte 23 is transmitted last.

Bit #	Access	Name	Description
31-16	-	-	Unused
15-8	W	CHACS	Channel B channel status data
7-0		CHACS	Channel A channel status data

Reset Value:
ChStat: undefined

5.2.9 Transmit sample data – Description

Format of data words in transmit sample buffer. Channel A is transmitted first, and must be stored on even addresses, while channel B is stored on odd addresses in the sample buffer.

Bit #	Access	Name	Description
31-24	-	-	Unused
23-16	W	DATH	Audio data if >16bit resolution. Unused bits are 0
15-0		DATL	Audio data (16bit mode). Bit 0 is LSB.

Reset Value:

Sample buffer: undefined

6

Clocks

The SPDIF interface uses only the Wishbone interface clock.

Name	Source	Rates (MHz)			Remarks	Description
		Max	Min	Resolution		
wb_clk_i	-	-		-	Must be at least 8 times higher than SPDIF data rate	System clock.

Table 6: List of clocks

7

IO Ports

7.1 Wishbone interface signals (receiver & transmitter)

Port	Width	Direction	Description
wb_ack_o	1	Output	Bus cycle acknowledge
wb_adr_i	8-64	Input	Address bus
wb_bte_i	2	Input	Burst type extension
wb_clk_i	1	Input	Clock
wb_cti_i	3	Input	Cycle type identifier
wb_cyc_i	1	Input	Valid bus cycle
wb_dat_i	16/32	Input	Data to core
wb_dat_o	16/32	Output	Data from core
wb_rst_i	1	Input	Asynchronous reset
wb_sel_i	1	Input	Select Input
wb_stb_i	1	Input	Strobe
wb_we_I	1	Input	Write enable

Table 7: Wishbone signals

Description	Specification
General description	16/32bit slave
Supported cycles	SLAVE, READ/WRITE SLAVE, BLOCK READ/WRITE SLAVE, Incrementing burst cycle (linear)
Data port, size Data port, granularity Data port, maximum operand size Data transfer ordering Data transfer sequencing	16 or 32bit 16 or 32bit 16 or 32bit Big/little endian Undefined

Wishbone properties

7.2 SPDIF Receiver signals

Port	Width	Direction	Description
spdif_rx_i	1	Input	SPDIF bi-phase encoded input signal
rx_int_o	1	Output	Interrupt signal (active high)

Table: Receiver signals

7.3 SPDIF Transmitter signals

Port	Width	Direction	Description
spdif_tx_o	1	Output	SPDIF bi-phase encoded output signal
tx_int_o	1	Output	Interrupt signal (active high)

Table: Transmitter signals